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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,783	06/19/2006	Brendan P. Kelly	GB03 0080 US	5854

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EXAMINER	
VELEZ, ROBERTO	

ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
04/24/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/561,783	KELLY, BRENDAN P.	
	Examiner	Art Unit	
	Roberto Velez	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 4-5 are objected to because of the following informalities: Claim 4, line 1 recites "A semiconductor device according...". To keep consistency in claim language with the preamble of previous claims, claim 4, line 1 should recite "A power semiconductor device according...". Similar changes are required for claim 5. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmoock et al. (US Pat 6,624,994) in views of Valley (US Pat. 4,743,779) and Applicant's Admitted Prior Art Fig. 1 (herein after AAPA).

Regarding claim 1, Schmoock et al. shows (Fig. 2) a power semiconductor device, comprising: an output transistor [52, 32] having main cells [32] and sense cells [52]; a control input (connection from 58 to gate of 52) connected to the main [32] and sense cells [52] and main and sense cell controlled outputs (drain and source of each 52 and 32); an output terminal [V_{out}] connected to one of the main cell [32] controlled outputs (source) for connection to a load (Col. 4, Ln 45-48); a feedback circuit [V_{ref}, 44, 48] for measuring the voltage across the main cell controlled outputs (drain and source)

of the output transistor and controlling (through 48) the voltage on the control input (Col. 5, Ln 47-53); a reference current supply [54] feeding a reference current through the sense cell [52] controlled outputs (Col. 6, Ln 55-57); and a comparator [40] arranged to compare the voltages across the main cell outputs (drain and source of 52) and the sense cell outputs (drain and source of 32).

Schmoock et al. fails to disclose a feedback circuit for increasing the voltage across the main cell controlled outputs if the magnitude of the voltage across the controlled outputs falls below a predetermined value. However, Valley shows (Fig. 1) a feedback circuit [100 and 50] for increasing or decreasing the voltage across the circuit controlled outputs if the magnitude of the voltage across the controlled outputs falls below or above a predetermined value (Col. 3, Ln 26-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Valley into the device of Schmoock et al. by providing a feedback circuit configured to increase the voltage across the main cell controlled outputs if the magnitude of the voltage across the controlled outputs falls below a predetermined value. The ordinary artisan would have been motivated to modify Schmoock et al. in the manner set forth above for the purpose of maintaining the power semiconductor device operating at a desired range to avoid damaging the circuitry of the power semiconductor device.

The combination of Schmoock et al. and Valley fails to disclose a comparator arrange to output a low-current signal when the magnitude of the voltage across the main cell outputs falls below that across the sense cell outputs. However, AAPA shows

(Fig. 1) a comparator [18] arrange to output a low-current signal when the magnitude of the voltage across the cell outputs falls below a value (Page 1, Ln 28-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of AAPA into the device of the combination of Schmoock et al. and Valley by providing a comparator arranged to output a low-current signal when the magnitude of the voltage across the main cell outputs falls below that across the sense cell outputs. The ordinary artisan would have been motivated to modify the combination of Schmoock et al. and Valley in the manner set forth above for the purpose of monitoring the operation of the main cell and the sense cell in order to detect a fault.

Regarding claim 2, the combination of Schmoock et al., Valley and AAPA discloses everything as claimed above in claim 1; in addition, Schmoock et al. shows (Fig. 2) wherein the feedback circuit [V_{ref}, 44, 48] includes a voltage reference [V_{ref}] and a comparator [44] connected across the main cell outputs (drain and source of 32) for comparing the voltage across the main cell outputs (drain and source of 32) with the voltage reference [V_{ref}] (Col. 5, Ln 25-30).

Schmoock et al. fails to disclose the output of the comparator being connected through a diode to the control input, the diode being orientated to pass current to change the control voltage in a direction to increase the on-resistance of the main cells when the voltage across the main cell outputs fails below the predetermined value. However, Valley shows (Fig. 1) the output of the comparator [100] being connected through a diode [96], the diode [96] being orientated to pass current to change the

control voltage in a direction to increase the on-resistance of the circuit when the voltage across the circuit outputs fails below the predetermined value (Col. 3, Ln 44-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Valley into the device of the combination of Schmoock et al. and AAPA by connecting the output of the comparator through a diode to the control input, the diode being orientated to pass current to change the control voltage in a direction to increase the on-resistance of the main cells when the voltage across the main cell outputs fails below the predetermined value. The ordinary artisan would have been motivated to modify the combination of Schmoock et al. and AAPA in the manner set forth above for the purpose of controlling the flow of current from and into the comparator and the main cell to avoid transmitting erroneous voltages that could damage the power semiconductor device.

Regarding claim 3, the combination of Schmoock et al., Valley and AAPA discloses everything as claimed above in claim 1; in addition, Schmoock et al. shows (Fig. 2) a power semiconductor transistor according to claim 1 wherein the main [32] and sense [52] cells are FET main and sense cells and the gates of the FETs are connected in common to the control input and the sources and drains of the FETs of the main and sense cells form the outputs of the FETs.

Regarding claim 4, the combination of Schmoock et al., Valley and AAPA discloses everything as claimed above in claim 3; in addition, Schmoock et al. shows (Fig. 2) in the form of a high side device wherein: the drains of the sense and main cells [52, 32] are connected in common to a battery terminal the source [V_{in}] of the main cells

is connected to the output terminal and the source of the sense cells is connected to the reference current [54] supply, the reference current supply [54] being a reference current sink.

Regarding claim 5, the combination of Schmoock et al., Valley and AAPA discloses everything as claimed above in claim 1; in addition, Schmoock et al. shows (Fig. 2) a power semiconductor device including a semiconductor device (52 and 32 are semiconductor devices according to claim 1 further comprising a load (connected to V_{out}) connected to the output terminal [V_{out}] (Col. 4, Ln 45-48).

Regarding claim 6, Schmoock et al. shows (Fig. 2) a method of operating a semiconductor device, the device including an output transistor [52, 32] having main cells [32] and sense cells [52]; and a control input (connection from 58 to gate of 52) connected to the main [32] and sense cells [52] and main and sense cell controlled outputs (drain and source of each 52 and 32), the method including: driving (using V_{in}) the main and the sense cells [52, 32] in common; driving a load (connected in V_{out}) from one of the main cell [32] controlled outputs; feeding (using 54) a reference current through the sense cell [52] controlled outputs (Col. 6, Ln 55-57); measuring (using 44) the voltage across the main cell controlled outputs (drain and source) and controlling (through 48) the voltage on the control input (Col. 5, Ln 47-53); and comparing (using 40) the voltages across the main cell controlled outputs (drain and source of 52) and the sense cell controlled outputs (drain and source of 32).

Schmoock et al. fails to disclose increasing the voltage across the main cell controlled outputs if the magnitude of the voltage across the controlled outputs falls

below a predetermined value. However, Valley shows (Fig. 1) a feedback circuit [100 and 50] for increasing or decreasing the voltage across the circuit controlled outputs if the magnitude of the voltage across the controlled outputs falls below or above a predetermined value (Col. 3, Ln 26-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Valley into the device of Schmoock et al. by providing a feedback circuit configured to increase the voltage across the main cell controlled outputs if the magnitude of the voltage across the controlled outputs falls below a predetermined value. The ordinary artisan would have been motivated to modify Schmoock et al. in the manner set forth above for the purpose of maintaining the power semiconductor device operating at a desired range to avoid damaging the circuitry of the power semiconductor device.

The combination of Schmoock et al. and Valley fails to disclose outputting a low-current signal when the magnitude of the voltage across the main cell outputs falls below that across the sense cell outputs. However, AAPA shows (Fig. 1) a comparator [18] arrange to output a low-current signal when the magnitude of the voltage across the cell outputs falls below a value (Page 1, Ln 28-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of AAPA into the device of the combination of Schmoock et al. and Valley by providing a comparator arranged to output a low-current signal when the magnitude of the voltage across the main cell outputs falls below that across the sense cell outputs. The ordinary artisan would have

been motivated to modify the combination of Schmoock et al. and Valley in the manner set forth above for the purpose of monitoring the operation of the main cell and the sense cell in order to detect a fault.

Regarding claim 7, the combination of Schmoock et al., Valley and AAPA discloses everything as claimed above in claim 6; in addition, Schmoock et al. shows (Fig. 2) wherein the step of measuring the voltage across the main cell controlled outputs is performed by: comparing (using 44) the voltage across the main cell controlled outputs (drain and source of 32) with a reference voltage [V_{ref}] using a comparator [44] (Col. 5, Ln 25-30).

Schmoock et al. fails to disclose driving the control input from the output of the comparator through a diode, the diode being orientated to pass current to change the control input voltage in a direction to increase the on-resistance of the main cells when the voltage across the main cell outputs falls below the predetermined value. However, Valley shows (Fig. 1) the output of the comparator [100] being connected through a diode [96], the diode [96] being orientated to pass current to change the control voltage in a direction to increase the on-resistance of the circuit when the voltage across the circuit outputs falls below the predetermined value (Col. 3, Ln 44-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Valley into the device of the combination of Schmoock et al. and AAPA by connecting the output of the comparator through a diode to the control input, the diode being orientated to pass current to change the control voltage in a direction to increase the on-resistance of the main cells

when the voltage across the main cell outputs fails below the predetermined value. The ordinary artisan would have been motivated to modify the combination of Schmoock et al. and AAPA in the manner set forth above for the purpose of controlling the flow of current from and into the comparator and the main cell to avoid transmitting erroneous voltages that could damage the power semiconductor device.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Szepesi (US Pat. 5,018,041) discloses a circuit for internal current limiting in a fast high side power switch.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-272-8597. The examiner can normally be reached on Monday-Friday 8:00am- 4:30 pm.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Roberto Velez/
Examiner, Art Unit 2829
04/16/2008

/Ha T. Nguyen/

Supervisory Patent Examiner, Art Unit 2829